QP Code	1	6	0	1	0	8	Register Number								

VELALAR COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Semester Examinations – April / May 2017 Regulations-2016

Programme: ME-VLSI Design Semester: 2 Max. Marks: 100 Duration 3 Hrs

Course Code & Title: **16VLE04 ADVANCED DIGITAL LOGIC SYSTEM DESIGN**

Knowledge Levels (KL)	K1 - Remembering	K3 - Applying	K5 – Evaluating
	K2 - Understanding	K4 – Analyzing	K6 – Creating

Part A - Answer ALL Questions. 10 x 2 = 20 Marks

No.	Question	KL
1.	Differentiate between Combinational and Sequential circuits.	K2
2.	State the need for ASM Charts.	K1
3.	What is meant by Races?	K1
4.	State the effects of hazards in asynchronous sequential circuits.	K1
5.	Show fault table for two input NAND gate.	K4
6.	State any two properties of Boolean difference method.	K1
7.	List out the reasons for system failure.	K1
8.	Define system integrity.	K1
9.	Draw the timing diagram of the read cycle of static RAM.	K2
10.	Differentiate between CPLD and PAL.	K2

Part B - Answer ALL Questions. 5 x 13 = 65 Marks

No			Question	Marks	KL
11.	a		Design a serial adder using Mealy model and Moore model. Also draw the ASM Chart for the both models.	13	K6
			OR		
	b		Design a 5 bit Array multiplier with suitable diagrams.	13	K5
12.	a		Explain the flow reduction table with an example.	13	K2
			OR		
	b		Describe in detail about the various types of hazards in the asynchronous sequential circuit.	13	K1
13.	a	i.	Explain the path sensitization method with an example.	7	K2

		ii.	Estimate the Kohavi algorithm with an example.	6	K2
			OR		
	b		Explain the Built-in self-test (BIST) with neat diagram.	13	K2
14.	a	i.	Discuss the method of estimating the system reliability.	7	K2
		ii.	Explain how reflections should occur at both ends of a transmission line.	6	K2
			OR		
	b		Explain in detail about the various formal verifications of digital system.	13	K2
15.	a		Describe in detail about the internal architecture of logic analyzer and functionality.	13	K1
			OR		
	b		Explain in detail about the timing analysis of synchronous static RAM and dynamic RAM functions.	13	K2

Part-C **1 x 15 = 15 Marks**

16.	a	Design a Mod 5 counter using JK flip flop.	15	K6
		OR		
	b	Design an asynchronous sequential circuit, that has two inputs x_1 and x_2 and one output 'z'. The output z='1' when the sequence 00,01,11 is produced. Design using D-FF.	15	K6

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