| QP Code | 1 | 6 | 0 | 0 | 9 | 4 | Register Number | | | | | | | | |
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# VELALAR COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Semester Examinations – April / May 2017 Regulations-2016

Programme: M.E-VLSI Design Semester: 2 Max. Marks: 100 Duration 3 Hrs

Course Code & Title: **16VLE04 DSP INTEGRATED CIRCUITS**

| Knowledge Levels (KL) | K1 - Remembering | K3 - Applying | K5 – Evaluating |
|---|---|---|---|
| | K2 - Understanding | K4 – Analyzing | K6 – Creating |

**Part A - Answer ALL Questions. 10 x 2 = 20 Marks**

| No. | Question | KL |
|---|---|---|
| 1. | Differentiate application specific signal processor with algorithmic specific signal processor. | K2 |
| 2. | Draw nMOS inverter and nMOS NAND gate. | K3 |
| 3. | A signal $x(t) = 2\sin(5\pi t)$ is sampled at sampling frequency of $F_S$ = 10Hz. Justify that signal can be reconstructed from its discrete samples. | K5 |
| 4. | Support that FFT can be faster than DFT. | K5 |
| 5. | Justify that 'Number of arithmetic operations are less in Half-Band FIR filters'. | K5 |
| 6. | Specify the measuring method of round-off noise. | K1 |
| 7. | Distinguish multiprocessor and multicomputer. | K4 |
| 8. | Relate throughput per unit chip area with cost of shared-memory. | K3 |
| 9. | Change the Two's complement number($(0.00111100)_{2C}$ ) into CSDC number. | K3 |
| 10. | Calculate the reduced memory word where original memory word is 1024 words using memory size reduction technique. | K3 |

**Part B - Answer ALL Questions. 5 x 13= 65 Marks**

| No | | | Question | Marks | KL |
|---|---|---|---|---|---|
| 11. | a | | Describe the top-down approach, Bottom up approach, Edge in approach and Meet in the middle approach in partition techniques. | 13 | K2 |
| | | | OR | | |
| | b | | Compare and explain GaAS technology with BICMOS, SOI, ECL and TTL technologies. Besides prove that power consumption of GaAS technology is lower than ECL & TTL logics. | 13 | K4 |
| 12. | a | i | Point out the suitable method to generate adaptive filter coefficients. | 8 | K4 |
| | | ii | Select and discuss the sample frequency to avoid aliasing effect in sampling process. | 5 | K2 |
| | | | OR | | |

| | | | | | |
|---|---|---|---|---|---|
| | b | | Compare different types of discrete cosine transforms with their appropriate equations. | 13 | K2 |
| 13. | a | i | Correlate the linear-phase FIR filter with Half-Band FIR filters in detail. | 8 | K4 |
| | | ii | Choose the mapping function for analog transfer function into digital function in IIR system. | 5 | K6 |
| | | | OR | | |
| | b | i | Design a system for interpolation of sample frequency by a factor of 163/127 and 149/77. | 8 | K4 |
| | | ii | Explain interpolation with an integer factor L in Frequency domain. | 5 | K2 |
| 14. | a | i. | Compare vector – multiplier based implementation and numerically equivalent implementation in detail. | 8 | K2 |
| | | ii. | Distinguish systolic and wavefront arrays. | 5 | K5 |
| | | | OR | | |
| | b | | Discuss about shared memory architecture with Bit-serial PEs. | 13 | K2 |
| 15. | a | | Discriminate five carry adders to reduce the switching operation in carry propagation. Also explain basic shift-add multiplication. | 13 | K5 |
| | | | OR | | |
| | b | | Illustrate in detail about Booth, Wallace tree & Baugh-Wooley's multipliers. | 13 | K5 |

**Part-C** **1 x 15 = 15 Marks**

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|---|---|---|---|---|---|
| 16. | a | | Conclude that computational complexity of Discrete Fourier transform can be reduced by Cooley-Tukey method and Sande-Tukey FFT with proper examples. | 15 | K5 |
| | | | OR | | |
| | b | | Choose a suitable method for measurement of FFT round off noise in a digital system. Discuss Parasitic oscillations in detail. | 15 | K5 |

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