QP Code	1	6	0	0	9	6	Register Number								

VELALAR COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Semester Examinations – April / May 2017 Regulations-2016

Programme: ME-AE/VLSI Design Semester: 2 Max. Marks: 100 Duration 3 Hrs

Course Code & Title: **16VLT22/ 16AEE08** **LOW POWER VLSI DESIGN**

Knowledge Levels (KL)	K1 - Remembering	K3 - Applying	K5 – Evaluating
	K2 - Understanding	K4 – Analyzing	K6 – Creating

Part A - Answer ALL Questions. 10 x 2 = 20 Marks

No.	Question	KL
1.	Identify the various sources of power consumption in CMOS circuits.	K2
2.	Mention the condition for reverse short channel effect.	K2
3.	List out the methods to reduce the dynamic power dissipation.	K1
4.	Define short circuit and dynamic dissipation.	K1
5.	List out the methods to reduce clock power consumption.	K1
6.	Write the salient features of adiabatic logic.	K2
7.	Large improvements in power dissipation are possible only at higher levels of design abstraction. Why?	K4
8.	Indicate the needs of architectural level power estimation methods.	K3
9.	State the sources of software power dissipation.	K1
10.	Point out two algorithm level techniques for low power dissipation.	K4

Part B - Answer ALL Questions. 5 x 13 = 65 Marks

No		Question	Marks	KL
11.	a	Explain about the design limitations imposed on low power, low voltage circuits pertaining to the following parameters. (i) Power Supply Voltage (ii) Threshold voltage (iii) Scaling (iv) Interconnect Wires	(03) (03) (03) (04)	K2
		OR		
	b	Derive the threshold voltage equation and the effects influencing threshold voltage in sub-micron MOSFET Physics.	13	K4

12.	a		With neat CMOS Circuit and examples, explain the evaluation procedure of dynamic power consumption in dynamic flip flop.	13	K2
			OR		
	b	i.	Analyze logic level optimization using FSM and Combinational logic synthesis.	7	K4
		ii.	Discuss the characterization and power consumption of CMOS gates.	6	K2
13.	a		Explain the interconnect and layout design techniques for low power design.	13	K2
			OR		
	b		Explain the power reduction method in various stages of sense amplifier circuits of SRAM.	13	K2
14.	a		Draw and Explain the flow chart of Monte Carlo based technique for estimation of average power in sequential circuits.	13	K4
			OR		
	b		Explain logic level power estimation techniques in detail.	13	K2
15.	a	i.	Explain the concept of pre consumption logic for reducing power.	7	K2
		ii.	Elaborate the use of pipelining and parallelism.	6	K1
			OR		
	b		Write short notes on		
			(1) Power optimization using operation equation.	7	K2
			(2) Architecture driven voltage scaling.	6	
			Part-C	**1 x 15 = 15 Marks**	
16.	a		With neat sketch illustrate in detail about the following CMOS Logic Circuits. a) Pass transistor logic b) Differential Voltage Logic Styles c) Push-Pull pass transistor logic.	15	K5
			OR		
	b.		Design and analyze a 4-bit ripple carry adder and compare its area, delay and power using different logic styles.	15	K5

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