QP Code	1	6	0	0	9	3	Register Number								

VELALAR COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Semester Examinations – April / May 2017 Regulations-2016

Programme: ME-VLSI Semester: 2 Max. Marks: 100 Duration 3 Hrs

Course Code & Title: **16VLT23 SYSTEM ON CHIP DESIGN**

Knowledge Levels (KL)	K1 - Remembering	K3 - Applying	K5 – Evaluating
	K2 - Understanding	K4 – Analyzing	K6 – Creating

Part A - Answer ALL Questions. 10 x 2 = 20 Marks

No.	Question	KL
1.	State the properties of Logic Gates.	K4
2.	How will you analyze the performance of logic gate using multiple threshold logic MTCMOS.	K4
3.	List out the types of simulators used for combinational logic design.	K1
4.	Mention the effects of transistor sizing.	K2
5.	State the differences between Latches and Flip-flops.	K2
6.	How will you optimize the power in sequential systems?	K4
7.	Draw the structure of a pipelined system and state the latency of a pipeline and pipeline depth.	K3
8.	Mention the difference between a ripple carry adder and carry select adder.	K2
9.	Specify the importance of Floorplaing and also list the various Floorplaning Techniques.	K1
10.	List the different ways to improve clock distribution.	K4

Part B - Answer ALL Questions. 5 x 16 = 80 Marks

No			Question	Marks	KL
11.	a	i.	Construct the NAND and NOR static complementary gates and explain.	6	K6
		ii.	Draw the layout of NAND gate.	7	K1
			OR		
	b		Analyze the delay through resistive interconnects with suitable circuits.	13	K4
12.	a	i.	Explain how to design logic networks using Interconnect models.	7	K3
		ii.	With suitable circuit, explain the significance of fanout and path delay in maximizing the system performance.	6	K1

OR

	b	i.	How will you test a logic gates? Explain the various models used to consider the effects of faults.	6	K4
		ii.	How to optimize the power consumption of an isolated logic gate?	7	K4
13.	a		With suitable system structure explain the sequential systems and clocking disciplines.	13	K1
			OR		
	b	i.	With suitable state transition graph and tables analyze the structural specification of a counter.	7	K4
		ii.	Explain in detail about the sequential testing.	6	K1
14.	a	i.	Draw the structure of a barrel shifter and explain how a barrel shift performs shift and rotate operation	6	K5
		ii.	Construct a serial parallel multiplier and evaluate the performance of the system.	7	K5
			OR		
	b	i.	Sketch the architecture of high density memory and explain it in detail.	7	K2
		ii.	Explain about the organization of PLA.	6	K1
15.	a	i.	Explain about Block placement and channel definition in floor planning.	7	K2
		ii.	Is it necessary to go through the placement-global routing cycle several times? Justify your answer.	6	K2
			OR		
	b		Illustrate in detail about the Off chip connections and state the role of a chip designer.	13	K2

Part C **1 x 15 = 15 Marks**

16.	a.	Draw the stick diagram for a 1-bit multiplexer cell built from static complementary gates.	15	K6
		OR		
	b.	Design the static complementary pull-ups and pull-down for these Logic expressions.	15	K5

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